REMARKS

The Final Office Action mailed December 23, 2002, has been received and reviewed. Claims 1 through 14 are currently pending in the application. Claims 1 through 14 stand rejected. Applicants propose to amend Claims 3, 6, and 8 and respectfully request reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 112 Claim Rejections

Claims 12 and 14 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

Paragraph **[0012]** states, "When one or more dice on a memory module are found defective, one or more replacement chips can be attached to the one or more auxiliary chip attach locations with the size of the replacement chips being at least equal to the amount of defective memory. Thus, the defective dice can be replaced without needing to be physically removed. Moreover, by providing auxiliary chip attach locations that can accept different sizes and memory capacities of replacement semiconductor chips, one replacement chip can replace several defective chips on the memory module."

Paragraph **[0013]** states, "Thus, depending on the amount of defective memory detected on the SIMM, a replacement chip having at least that amount of good memory can be attached to the auxiliary chip attach location."

Paragraph **[0033]** states, "As illustrated in FIG. 3, however, if more than one chip 14 fails or memory equaling the capacity of more than one chip is proven defective during burn-in, it may be necessary to connect a larger-capacity replacement chip 50 to the auxiliary chip attach location, one that provides enough memory to replace the combined memory of the failed chips 14."

Paragraph **[0039]** states, "Accordingly, depending on the number, if any, of defective or bad chips 116, various combinations of known-good replacement chips can be selected

depending on the size and memory size of those on hand."

Claim 12 recites at least one additional memory chip providing an amount of functional memory substantially equal to said amount of nonfunctional memory collectively exhibited by said plurality of memory chips.

Claim 14 recites at least one additional memory chip providing an amount of functional memory substantially equal to said amount of nonfunctional memory collectively exhibited by said plurality of memory chips.

Accordingly, Applicants respectfully submit that Claim 12 and Claim 14 do not constitute new matter, as each of the claims fall within the specification as cited above. Applicants respectfully request reconsideration and withdrawal of 35 U.S.C. § 112 rejections to Claims 12 and 14.

Double Patenting Rejections

On page 3 of the Final Office Action, Examiner notes that a terminal disclaimer disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,008,538 filed on 11/13/02 has been recorded. However, allowance of Claims 1 and 2 is not noted on the Office Action Summary.

Since a terminal disclaimer has been timely filed and recorded and no additional grounds for rejection of claims 1 and 2 are recited in the outstanding Office Action, Applicants respectfully request an indication of the allowance of Claims 1 and 2.

35 U.S.C. § 102(a) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,502,333 to Bertin et al.

Claims 3 through 8, 10, 11 and 13 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Bertin et al., U.S. Patent No. 5,502,333, ("Bertin"). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Bertin discloses electronic semiconductor structures including a spare memory circuit. The memory circuit may comprise one or more substantially identical memory chips that essentially replace a "bad" chip. Alternatively, individual cells within chips may be replaced by "sparing" of a multichip package after encapsulation. (Col. 7, lines 53-58). Thus, Bertin et al. builds in some additional memory and completes fabrication of the module, relying on detection of nonfunctional memory and rerouting using logic to redundant memory already built in to the module in anticipation of some failures.

In the present invention, a site providing the *capability* of adding memory to replace memory found to be defective in case defective memory is exhibited upon testing. Thus, in the present invention, no "spare" chips or memory are added to the memory module unless and until some memory of the plurality of chips initially comprising the memory module are found to be defective. Further, the size of the chip or chips added may be selected upon testing of the memory module.

Bertin et al., as a result of the designs of the various embodiments thereof, does not appear to disclose "one or more additional locations on said substrate" configured to receive additional one or more additional chips. Instead, Bertin et al. builds in some additional memory and completes fabrication of the module prior to detection of nonfunctional memory. Then, Bertin discloses rerouting using logic to redundant memory already built in to the module in anticipation of some failures.

Claim 3, as presently amended, includes a programmable device configured to incorporate functional memory of one or more additional chips disposed at said one or more additional locations and selected in relation to an amount of detected nonfunctional memory of said plurality of memory chips on said substrate into said rerouted input and output paths. Applicants respectfully request reconsideration and allowance of Claim 3, as presently amended, as Bertin fails to disclose each and every element of the claim in as complete detail as is contained in the claim.

Claim 4 is allowable as depending from Claim 3, which is allowable. Applicants respectfully request reconsideration and allowance of Claim 4.

Claim 5 recites at least one additional memory chip containing at least some nonfunctional memory. Bertin, however, discloses that active semiconductor chips in a stack may be determined defective, subsequent to encapsulation and burn-in, and then a redundant semiconductor chip may be selected to replace the defective chip. (Col. 6, lines 15-37). Applicants respectfully submit that Bertin does not appear to disclose an additional memory chip having at least some nonfunctional memory because Bertin does not disclose testing such a chip for nonfunctional memory.

Further, even assuming, *arguendo,* that Bertin discloses a redundant chip that may have nonfunctional memory, there is no disclosure of such a chip mounted on at least one of said additional locations and operably coupled to said programmable device. Therefore, the disclosure of Bertin, at most, may simply indicate that the redundant chips are tested more rigorously than the other chips used in the stack prior to being used within the stack.

As to inherency of the redundant chip having nonfunctional memory, "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir.1993). At most, for argument's sake, Bertin discloses a mere probability that nonfunctional memory may occur in nonfunctional memory because Bertin relies on empirical yield data. (Col. 6, lines 29-33). Therefore, Applicants respectfully submit that the fact that nonfunctional memory may occur in the prior art is not sufficient to establish the inherency of that result.

The Examiner bears the burden to show and "must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art." M.P.E.P. §2112 (citing *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original)). Here, it appears that Bertin discloses replacement of a defective chip with a redundant chip which is not tested at any time whatsoever. Therefore, Applicants respectfully submit that Bertin does not necessarily disclose that the redundant chip contains nonfunctional memory.

Claim 5 is allowable as depending from Claim 3, which is allowable. Applicants respectfully request reconsideration and allowance of dependent Claim 5.

Claim 6 recites at least one additional memory chip comprising at least two memory chips having different memory capacity and being placed at different additional locations. Although Bertin, as cited by the Examiner, appears to disclose more than one redundant chip, Bertin does not appear to disclose redundant chips having differing memory capacities because Bertin discloses that the redundant chip is *identical* to the other chips. (Col.5, lines 37-42). Further, Examiner notes in the Final Office Action that Bertin does not show the spare chips as having different amounts of memory. (Page 5, paragraph 19). Again, Applicants respectfully submit that Bertin fails to disclose each and every element of the claim in as complete detail as is contained in the claim. Accordingly, Applicants respectfully request reconsideration and allowance of dependent Claim 6.

Claim 7 is allowable as depending indirectly from Claim 3, which is allowable. Applicants respectfully request reconsideration and allowance of Claim 7.

Independent Claim 8, as presently amended, recites at least one additional memory chip mounted to said substrate providing an amount of functional memory selected in relation to and equal to or greater than said amount of detected nonfunctional memory.

Applicants respectfully submit that Bertin does not disclose each and every element of the claim. Bertin discloses that redundant chips are placed without regard to detection of nonfunctional memory, and if nonfunctional memory exceeds the memory capacity of any one chip in the stack, multiple identical redundant chips are required. (Col. 6, lines 25-32). Thus, Bertin does not disclose selecting the redundant chips in relation to *detected* nonfunctional memory. Further, even assuming a cell replacement approach as disclosed by Bertin, Bertin expressly discloses that the number of cells n in a spare memory circuit is *less than or equal to* the number of cells m in each semiconductor chip. (Col. 3, lines 38-43). Thus, Bertin does not disclose providing an amount of functional memory selected in relation to and equal to or greater

than said amount of detected nonfunctional memory with regard to the replacement cell embodiment. Therefore, Bertin fails to disclose each and every element of independent Claim 8, as presently amended. Applicants respectfully request reconsideration and allowance of independent Claim 8.

Dependent Claims 10 and 11 each recite at least one additional memory chip containing an amount of functional memory substantially equal to an amount of nonfunctional memory in said at least one of said plurality of memory chips. Although Bertin discloses that active semiconductor chips in a stack may be determined defective, subsequent to encapsulation and burn-in, and then a redundant semiconductor chip may be selected to replace the defective chip. (Col. 6, lines 15-37). Accordingly, this embodiment of Bertin does not disclose each and every element of the claim because this replaces the functional memory of the defective chip as well as the nonfunctional memory. Further, Bertin discloses that the number of cells n in a spare memory circuit is less than or equal to the number of cells m in each semiconductor chip. Likewise, this embodiment of Bertin does not disclose each and every element of the claim. Moreover, dependent Claim 10 is allowable as indirectly depending from independent Claim 3, which is allowable. Dependent Claim 11 is also allowable as indirectly depending from independent Claim 3, which is allowable. Applicants respectfully request reconsideration and allowance of dependent Claims 10 and 11.

Dependent Claim 13 recites at least one additional memory chip containing at least some nonfunctional memory. Applicants respectfully submit that Bertin does not disclose each and every element of Claim 13, as outlined above with respect to Claim 5. Accordingly, Applicants respectfully request reconsideration and allowance of dependent Claim 13.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,502,333 to Bertin et al. in view of U.S. Patent No. 5,434,868 to Aichelmann, Jr. et al.

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,502,333 to Bertin et al. in view of U.S. Patent No. 5,434,868 to Aichelmann, Jr. et al. ("Aichelmann"). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim 9 are improper because the references, taken alone or in combination fail to teach or suggest all of the claim limitations.

Claim 9 recites at least one additional memory chip comprising at least two memory chips having different amounts of functional memory.

In the rejection, the Examiner acknowledges the Bertin reference is deficient in teaching two memory chips having different amounts of functional memory.

In addition, Aichelmann is deficient in teaching two memory chips having different amounts of functional memory. Aichelmann teaches that the spare pool could *consist* of 2×1 Meg *or* 4×1 Meg DRAMs. (Col. 4, lines 50-52) (Emphasis added). Also, Aichelman teaches that the present invention is not limited in any way to the particular *size* of the DRAM *chips* used in the memory or the spare pool. (Col. 4, lines 44-50) (Emphasis added). Therefore, Aichelman suggests that the chips used within the spare pool are all of a size, but that size may be selectable.

Claim 9 is allowable as depending from Claim 8, which is allowable. Applicants respectfully request reconsideration and allowance of Claim 9.

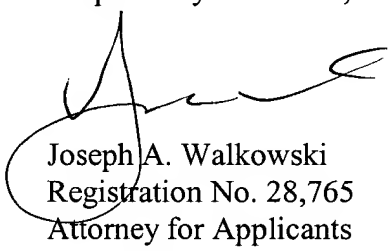
ENTRY OF AMENDMENTS

The proposed amendments to Claims 3, 6, and 8 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1-14 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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3. (Three Times Amended) A memory module, comprising:

a substrate having a plurality of memory chips [individually] mounted thereon; and

a programmable device adapted to reroute input and output paths to and from said plurality of memory chips to bypass nonfunctional memory in at least one of said plurality of memory chips, extending to one or more additional [individual] locations on said substrate and configured to incorporate functional memory of one or more additional chips disposed at said one or more additional [individual] locations and selected in relation to an amount of detected nonfunctional memory of said plurality of memory chips on said substrate into said rerouted input and output paths.

6. (Three Times Amended) The memory module of claim 4, wherein said at least one additional memory chip comprises at least two memory chips having different memory capacity and being placed at different additional [individual] locations.

8. (Three Times Amended) A memory module comprising:

a plurality of chips [individually] mounted to a substrate, said plurality of chips collectively exhibiting an amount of detected nonfunctional memory exceeding a memory capacity of any one chip of said plurality; and

at least one additional memory chip mounted to said substrate providing an amount of functional memory selected in relation to and equal to or greater than said amount of detected nonfunctional memory.